

TDA4601

SWITCH-MODE POWER SUPPLY CONTROLLER

- LOW START-UP CURRENT
- DIRECT CONTROL OF SWITCHING TRANSISTOR
- COLLECTOR CURRENT PROPORTIONAL TO BASE-CURRENT INPUT
- REVERSE-GOING LINEAR OVERLOAD CHARACTERISTIC CURVE

SIP9
(Plastic Package)

ORDER CODE : TDA4601

DIP 9+9
(Plastic Package)

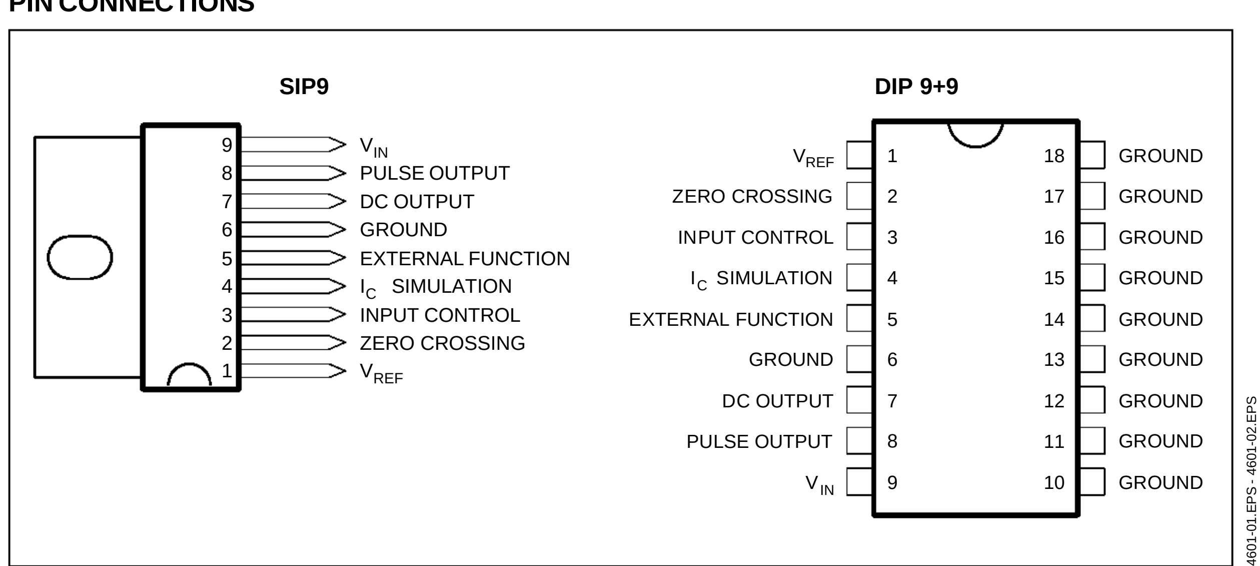
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DESCRIPTION

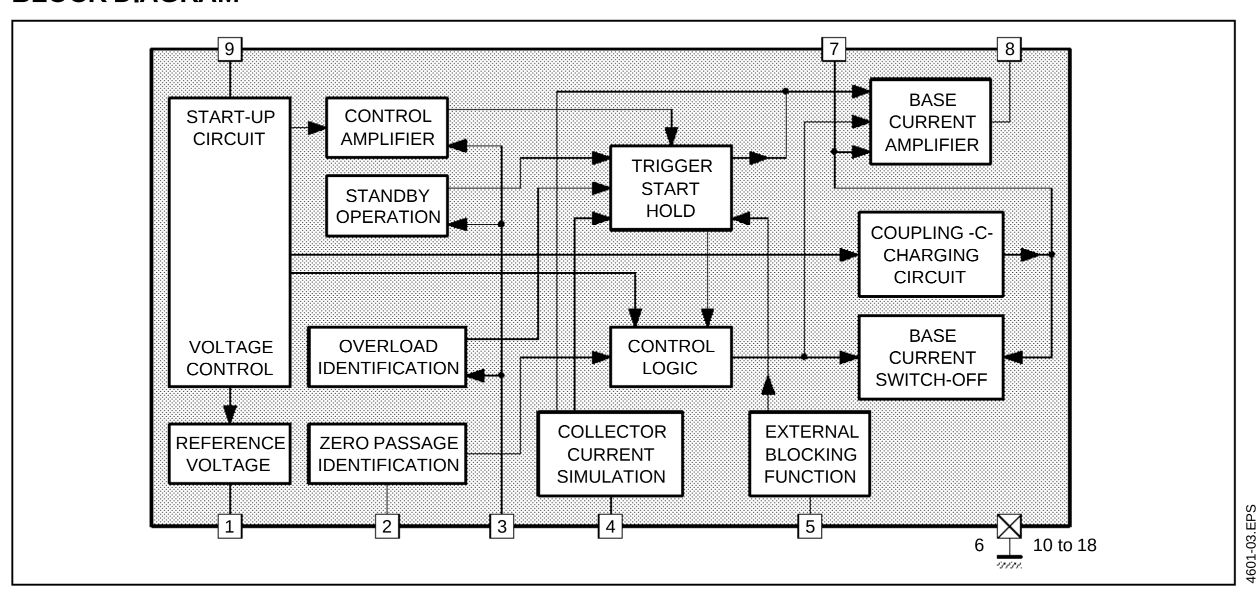
The TDA4601 is a monolithic integrated circuit desi-gned to regulate and control the switching transistor in a switching power supply.

Because of its wide operational range and high vol-tage stability even at high load changes, this IC can be used not only in TV receivers and video recorders but also in power supplies in Hi-Fi sets and active speakers.

PIN CONNECTIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_9	Supply Voltage	20	V
V_1	Reference Output	6	V
V_2	Identification Input	– 0.6, 0.6	V
V_3	Controlled Amplifier	3	V
V_4, V_5		8	V
V_7, V_8		V_9	
I_2, I_3		– 3, 3	mA
I_4		5	mA
I_5		5	mA
I_7		1.5	A
I_8		– 1.5	A
T_{oper}	Operating Ambient Temperature	0, 85	°C
T_{stg}	Storage Temperature	– 40, 150	°C
T_j	Junction Temperature	– 40, 125	°C

4601-01.TBL

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j–c)}$	Thermal Resistance Junction-pins	Max.	15	°C/W
$R_{th\ (j–a)}$	Thermal Resistance Junction–ambient	Max.	70	°C/W

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ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_9	Operating Supply Voltage Range		7.8		18	V
START CONDITION (according to test circuit of fig. 1)						
I_9	Supply Current (V_1 not yet switched on)	V_9 = 2 V V_9 = 5 V V_9 = 10 V		 1.5 2.4	0.5 2.0 3.2	mA mA mA
V_9	Switch Threshold (V_1)		11	11.8	12.3	V

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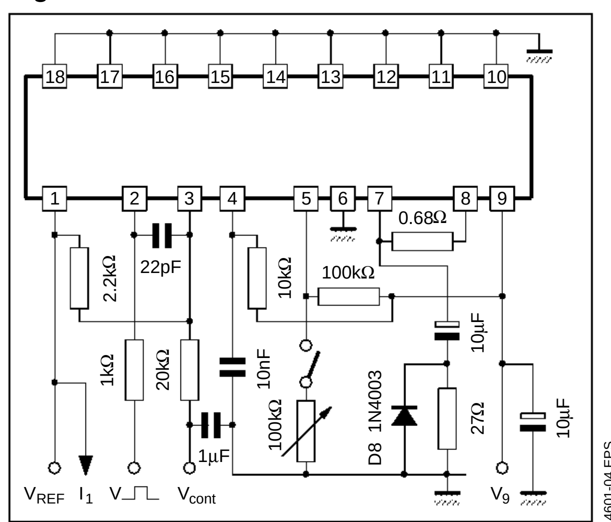
ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^oC$) (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
NORMAL OPERATION (V_9 = 10V, V_{cont} = – 10V, V_{clock} = ± 0.5V, f = 20kHz, duty cycle 1:2 after switch on)						
I_9	Supply Current	V_{cont} = – 10V V_{cont} = 0V	110 50	135 75	160 100	mA mA
V_{ref}	Voltage Reference at Pin 1	I_1 < 0.1mA I_1 = 5mA	4 4	4.2 4.2	4.5 4.4	V V
V_3	Control Voltage	V_{cont} = 0V	2.3	2.6	2.9	V
V_4	Collector Current Simulation Voltage	V_{cont} = 0V, see note 1	1.8	2.2	2.5	V
ΔV_4	Collector Current Simulation Voltage	V_{cont} = 0V to –10V, see note 1	0.3	0.4	0.5	V
V_5	External Protection Threshold		6	7	8	V
V_7	Pin 7 Output Voltage	V_{cont} = 0V, see note 1	2.7	3.3	4.0	V
V_8	Pin 8 output Voltage	V_{cont} = 0V, see note 1	2.7	3.4	4.0	V
ΔV_8	Pin 8 Output Voltage Change	V_{cont} = 0V to –10V, see note 1	1.6	2	2.4	V
V_2	Feedback Voltage	see note 1		0.2		V
T_{K1}	Reference Voltage Temperature Coefficient			10^{-3}		$1/^oK$
PROTECTION OPERATION (V_9 = 10V ; V_{cont} = – 10V ; V_{clock} = ± 0.5V ; f = 20kHz ; duty cycle 1 : 2)						
I_9	Supply Current	$V_5 \leq 1.8$ V	14	22	28	mA
V_7	Switch–off Voltage	$V_5 \leq 1.8$ V	1.3	1.5	1.8	V
V_4	Switch-off Voltage	$V_5 \leq 1.8$ V	1.8	2.1	2.5	V
V_5	Blocking Voltage	V_{cont} = 0 V	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
V_9	Supply Voltage for V_8 Blocked	V_{cont} = 0 V	6.7	7.4	7.8	V
ΔV_9	Supply Voltage for V_1 off While Further Decreasing V_9		0.3	0.6	1	V
ELECTRICAL CHARACTERISTICS (according to test circuit of fig. 2)						
t_{on}	Secondary Voltage Switching Time			350	450	ms
ΔV_2	Voltage Variation with Load	S_3 Closed, P_3 = 20 W		0.1	0.5	V
		S_2 Closed, P_2 = 15 W		0.5	1	V
ΔV_2	Stand by Condition	S_1 Open P_{load} = 3 W		20	30	V
f	Stand by Frequency		70	75		kHz
P_P	Primary Power Consumption in Stand by Condition			10	12	VA

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Note 1 : Only DC component

Figure 1 : Test Circuit



Test Diagram : Overload Operation

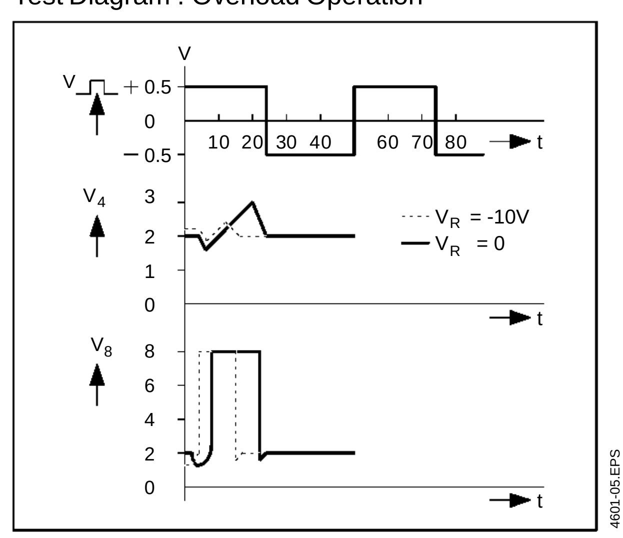


Figure 2 : Test and Application Circuit

(1) C limits the max. collector current of BU508 at overshooting the permissible output power.
(2) Adjustement of secondary voltage.
(3) Must be discharged before IC change.

CIRCUIT DESCRIPTION

The TDA 4601 regulates, controls, and protects the switching transistor in reverse converter power supplies at starting, normal, and overload operation.

Starting Behaviour

During the start-up, three consecutive operation states are passed.

1. An internal reference voltage is built up which supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. Up to a supply voltage of $V_9 \approx 12V$, the current I_9 is less than 3.2mA.
2. Release of the internal reference voltage $V_1 = 4V$. This voltage is abruptly available when $V_9 \approx 12V$ and enables all parts of the IC to be supplied from the control logic with a thermally stable and overload protected current supply.
3. Release of control logic. As soon as the reference voltage is available, the control logic is switched on through an additional stabilization circuit. Thus, the IC is ready for operation.

This start-up sequence is necessary to guarantee the supply through the coupling electrolytic capacitor to the switching transistor. Correct switching of the transistor is only guaranteed in this way.

Normal Operation

Zero crossing of the feedback coil is registered at pin 2 and passed to the control logic.

At pin 3 (regulation of input, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating amplifier works with an input voltage of about 2V and a current of about 1.4 mA.

Together with the collector current simulation pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at pin 4 and internally set threshold voltages. By increasing the capacitance (10nF) the max. collector current of the switching transistor rises, thus setting the required operating range. The extent of the regulation lies between a 2V clamped DC voltage and an AC voltage rising in a sawtooth waveform, which may vary up to a maximum amplitude of 4V (ref. voltage).

A reduction of the secondary load down to 20 watts causes the switching frequency to rise to about 50kHz at an almost constant pulse duty factor (period to on-time approx. 3). A further reduction of the secondary load down to about 1 watt results in changing the switching frequency to approx. 70kHz, and additionally the pulse duty factor rises to approx. 11. At the same time the collector peak current falls below 1A.

In the trigger the output level of the regulating amplifier, the overload recognition, and the collector current simulation are compared and instructions are given to the control logic. There is an additional triggering and blocking possibility by means of pin 5. The output at pin 8 is blocked at a voltage of less than 2.2V at pin 5.

Depending on the start-up circuit, the zero crossing identification, and the release with the aid of the trigger, the control logic flip flops are set which control the base current amplifier and the base current shut-down. The base current amplifier moves the sawtooth voltage V_4 to pin 8. A current feed-back having an external resistance of $R = 0.68\Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base driving current for the switching transistor.

Protective Measures

The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6V and thus blocks driving of the switching transistor. This protective measure will be released if the voltage at pin 9 reaches a value $\leq$ typ. 7.4V or if voltages of $\leq$ typ. 2.2V occur at pin 5. In the case of a short circuit of the secondary windings of the P.S.U., the IC continuously monitors the fault condition.

With the load completely removed from the secondary winding of the P.S.U., the IC is set to a low pulse duty factor. The total power consumption of the P.S.U. is held below 6 to 10 watts in both operating conditions. After having blocked the output, caused at a supply voltage $\leq$ typ. 7.4V, a further voltage reduction with $\Delta V_9 = 0.6V$ results in switching off the reference voltage (4V).

Figure 3 : Frequency versus Output Power (Test Circuit of Figure 2)

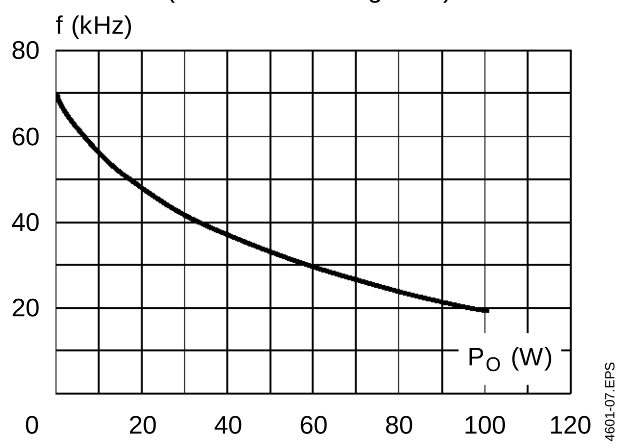


Figure 4 : Efficiency versus Output Power (Test Circuit of Figure 2)

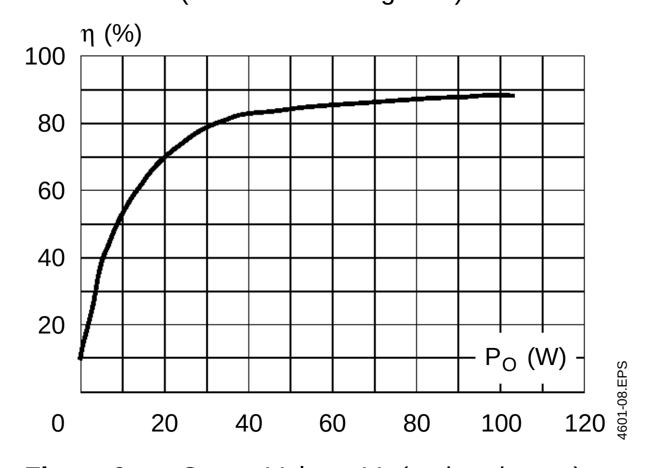


Figure 5 : Load Characteristics V_2-f (Iq2) (Test Circuit of Figure 2)

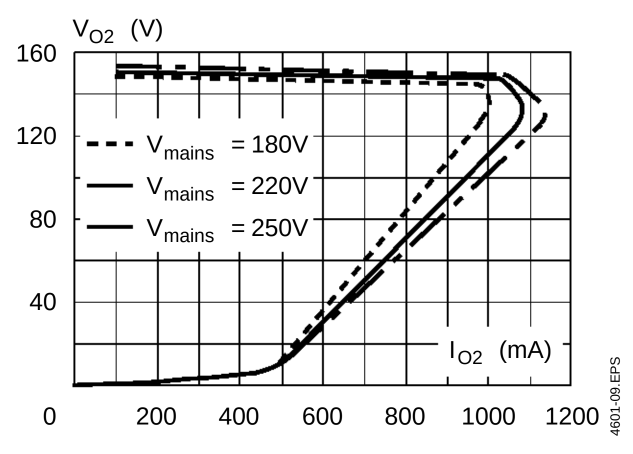


Figure 6 : Output Voltage V_2 (mains change) (Test Circuit of Figure 2)

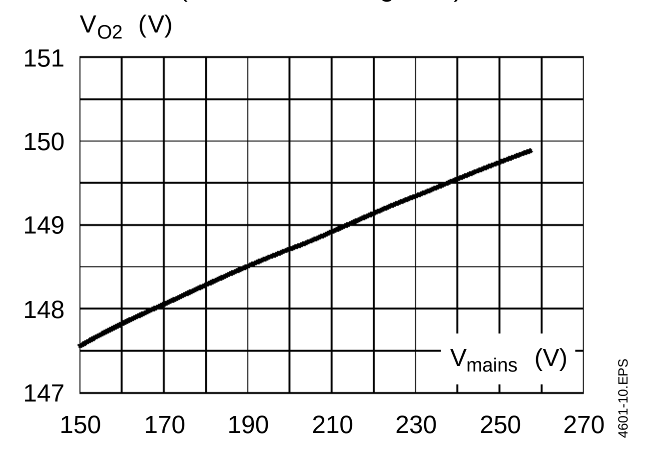
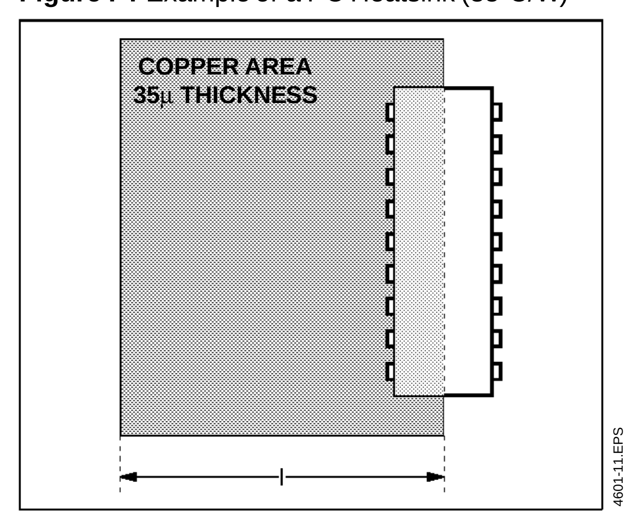
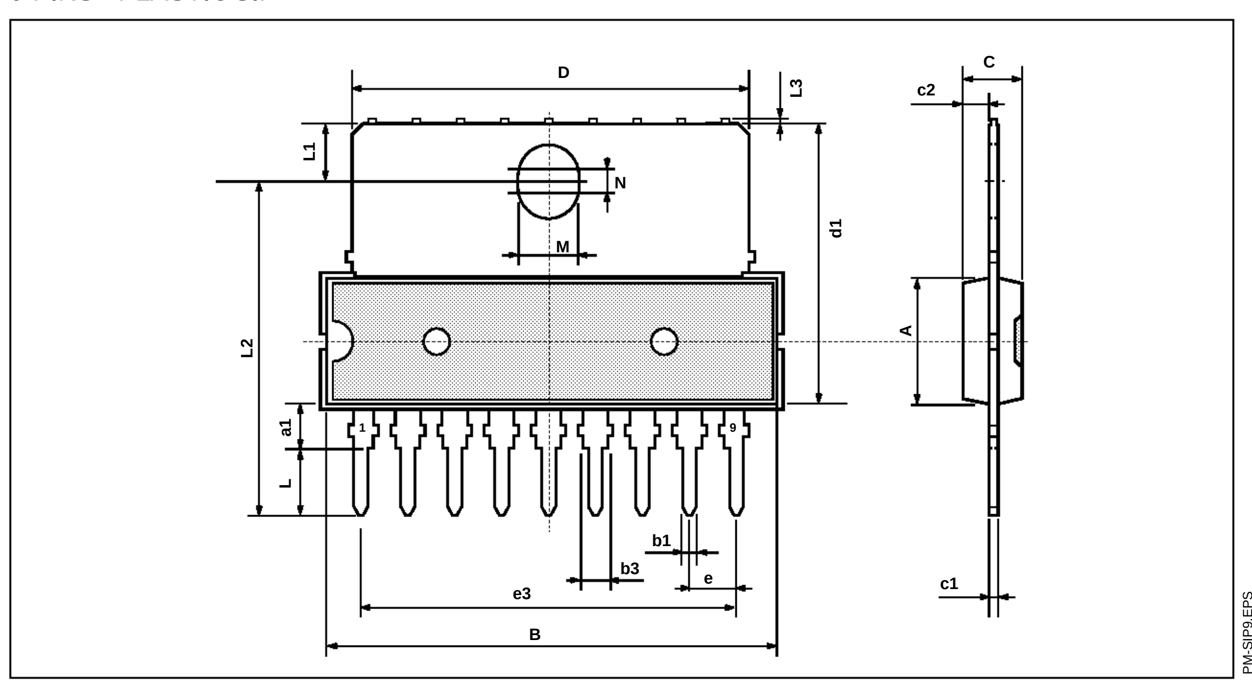


Figure 7 : Example of a PC Heatsink (35°C/W)



PACKAGE MECHANICAL DATA

9 PINS - PLASTIC SIP

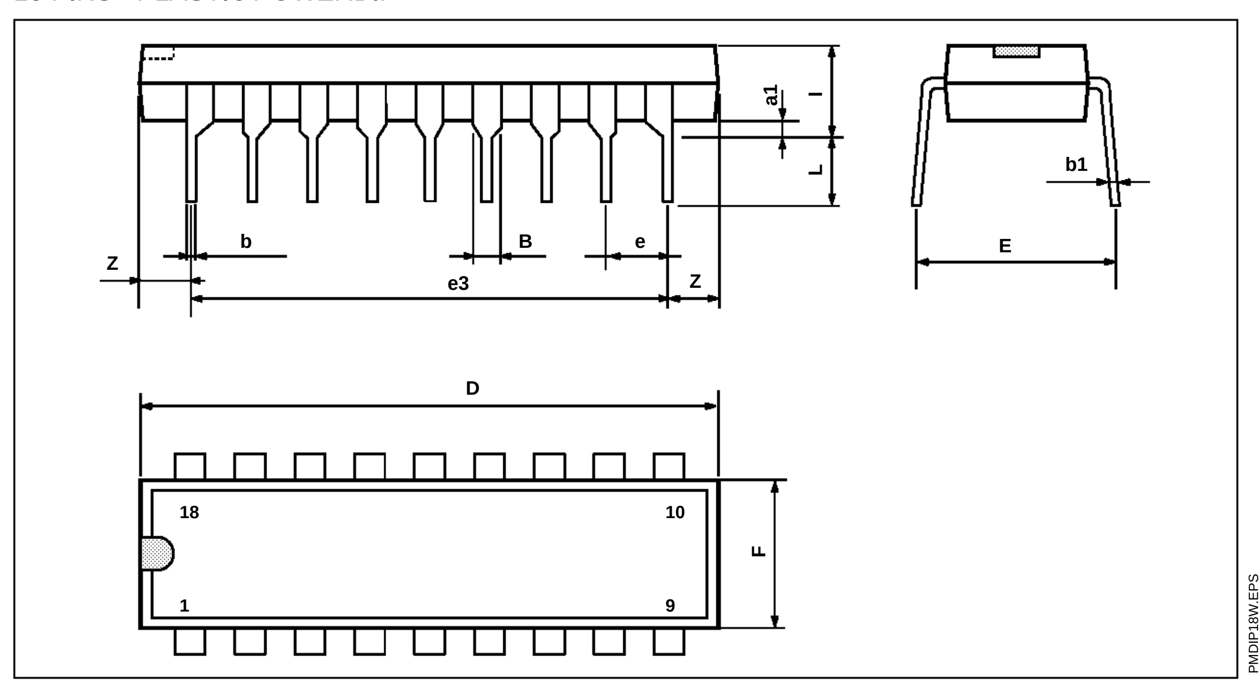


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

SIP9.TBL

PACKAGE MECHANICAL DATA

18 PINS - PLASTIC POWERDIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	0.85		1.4	0.033		0.055
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			24.8			0.976
E		8.8			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z			2.54			0.100

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